CLAIMS

What is claimed is:

1. A memory management method for error diffusion comprising the steps of:

dividing an image to be processed into a plurality of blocks;

filling an initial region of a block according to an error diffusion method;

performing error diffusion in order for each of the pixels in the block;

reserving the pixels that are not processed in the final region of the block to the next adjacent block; and

performing the error diffusion method for each of the blocks to complete halftone processing.

2. The method of claim 1, wherein the size of each divided block is smaller than the size of memory.

3. The method of claim 2, wherein the memory is an internal memory of an image processing chip.

4. The method of claim 3, wherein the internal memory is static random access memory (SRAM).

5. The method of claim 1, wherein the step of dividing an image to be processed into a plurality of blocks divides the image into a plurality of arrayed blocks.

6. The method of claim 5, wherein the arrayed blocks are regular rectangular blocks.

7. The method of claim 1, wherein the step of dividing an image to be processed into a plurality of blocks divides according to the error diffusion method.

8. The method of claim 7, wherein the block is an approximately zigzag shape.

9. The method of claim 1, wherein the step of filling an initial region of a block according to an error diffusion method filling the initial region of the block with required image data so that the pixels in the initial region are to be error diffused.

10. The method of claim 9, wherein the image data being filled are pixels that are not processed in its adjacent blocks.

11. The method of claim 9, wherein the image data being filled are empty pixels.

12. A halftone processing module for error diffusion for dividing an image into a plurality of blocks and using an error diffusion method to perform halftone processing, the module comprising:

an image processing chip, which executes the error diffusion;

an internal memory, which is inside the chip to store the block to be processed and the image data filling in the initial region of the block according to the error diffusion method for the image processing chip to process error diffusions; and

an external memory, which is outside the chip for providing the internal memory with the pixels needed to fill the block.

13. The halftone processing module of claim 12, wherein the internal memory is static random access memory (SRAM).

14. The halftone processing module of claim 12, wherein the block to be processed has an approximately zigzag shape according to the error diffusion method.

15. The halftone processing module of claim 12, wherein the image data filling in the initial region of the block are the image data that enable all the pixels in the initial region to

be error diffused according to the error diffusion method.

16. The halftone processing module of claim 15, wherein the filling image data are the pixels not processed in the adjacent blocks.

17. The halftone processing module of claim 16, wherein the pixels not processed are in the final region of the block.

18. The halftone processing module of claim 15, wherein the filling image data are empty pixels.

19. The halftone processing module of claim 12, wherein the external memory is dynamic random access memory (DRAM).